UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,776	09/30/2003	Jimmie Earl DeWitt JR.	AUS920030481US1	6262

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EXAMINER
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ART UNIT	PAPER NUMBER
2193	

NOTIFICATION DATE	DELIVERY MODE
01/21/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ptonotifs@yeeiplaw.com

	Application No.	Applicant(s)
	10/675,776	DEWITT ET AL.
Office Action Summary	Examiner	Art Unit	
	TUAN A. VU	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS,
WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on _30 September 2009_.

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) _1,6,26,29,30,32,34,35,38,39 and 49-53_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) _1, 6, 26, 29-30, 32, 34-35, 38-39, 49-53_ is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail. Date _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1.   This action is responsive to the Applicant's response filed 9/30/09.

       As indicated in Applicant's response, claims 1, 6, 26, 29-30, 32, 34-35, 38-39, 49-53

have been appealed. After reconsideration, the case is herein re-opened, and claims 1, 6, 26, 29-

30, 32, 34-35, 38-39, 49-53 are pending in the following Office Action.

Double Patenting

2.   The nonstatutory double patenting rejection is based on a judicially created doctrine

grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or

improper timewise extension of the "right to exclude" granted by a patent and to prevent possible

harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed.

Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686

F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA

1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

       A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to

overcome an actual or provisional rejection based on a nonstatutory double patenting ground

provided the conflicting application or patent is shown to be commonly owned with this

application. See 37 CFR 1.130(b).

       Effective January 1, 1994, a registered attorney or agent of record may sign a terminal

disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37

CFR 3.73(b).

3.   Claims 1, 32 are provisionally rejected under the judicially created doctrine of

obviousness-type double patenting as being unpatentable over claims 6, 21, 25 of copending

Application No. 10/675777 (hereinafter '777).

        Although the conflicting claims are not identical, they are not patentably distinct from

each other because of the following observations.

        As per instant claims 1, 32, '777 claims 6, 21, 25 also recite determining for a

instruction during execution for a association of an indicator associated with receiving a bundle

or instruction in a instruction cache; associating a counter based on such determination and

incrementing a counter in response to the indicator association with the instruction or event

associated with the indicator. The event counting and instruction cache as recited by '777 are

construed as obvious representation to a runtime indicator (leading to a counter increment, in

which incrementing is count of number of instructions execution) and sending from the cached

instruction for execution of the instant claims. Further, '777 does not recite 'spare bit' for

indicator identifying whether the instruction is to be monitored, but based on the indicator

received into a cache, a bit type implementation as a slot within an received instruction would

have been a obvious feature, enabling a monitoring to receive the instruction and increment a

counter based on '777 paradigm.

4.   Claims 1, 32 are provisionally rejected under the judicially created doctrine of

obviousness-type double patenting as being unpatentable over claims 2, 10, 20 of copending

Application No. 10/675778 (hereinafter '778). Although the conflicting claims are not identical,

they are not patentably distinct from each other because of the following observations.

As per claims 1, 32, '778 claims 2, 10, 20 recite receiving a instruction with an indicator generated from a instruction cache, wherein upon determining that an indicator is associated with an instruction and a signal from the cache instruction, incrementing the counter each time the instructions is executed based on said cache signal. Even though '778 does not recite receiving bundle into a instruction cache and sending the received bundle for execution, this limitation of instruction associated with indicator from cache would made the sending a obvious step within runtime based on instruction being cached in view of the above association and counting event.

Further, '778 does not recite 'spare bit' for indicator identifying whether the instruction is to be monitored, but based on the indicator received into a cache, a bit type implementation as a slot within an received instruction would have been a obvious feature, enabling a monitoring to receive the instruction and increment a counter based on '778 paradigm.

5.   Claims 1, 32 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 3, 17 of copending Application No. 10/675872 (hereinafter '872).

As per instant claims 1, 32, '872 claims 3, 17 also recite instruction to be monitored and sent from cache instruction, determining whether an instruction in execution is related with an runtime range 'indicator'; and counting each event associated with the instruction if the instruction is associated with that range indicator. Even though '872 does not recite receiving bundle into a instruction cache and sending the received bundle for execution, said limitation of instruction with associated indicator would made the instruction cache receiving and sending obvious steps within runtime based on instruction being cached in view of the above known concept, and the incrementing responsive to association of instruction with the indicator. Even

though '872 explicitly recites that the indicator is a location within contiguous range, this

location-within- range limitation would be a obvious representation of any runtime indicator that

would characterizes as an event deemed for the counter to be incremented (in which

incrementing in terms of count of number of instructions execution) in view of the above

association determination. Further, '872 does not recite 'spare bit' for indicator identifying

whether the instruction is to be monitored, but based on the indicator received into a cache, a bit

type implementation as a slot within an received instruction would have been a obvious feature,

enabling a monitoring to receive the instruction and increment a counter based on '872

paradigm.

6.   Claims 6, 34, 43 are provisionally rejected under the judicially created doctrine of

obviousness-type double patenting as being unpatentable over claims 4, 12, 20 of copending

Application No. 10/675721 (hereinafter '721).

   As per instant claims 6, 34, 43, '721 claims 4, 12, 20 also recite determining for a

instruction during execution for a association of a indicator, shadow memory (Note: even

though '721 does not recite counter in shadow memory per se, a set of indicators being sent for

monitoring would have made the counter as obviously in the shadow memory); incrementing a

counter in response to the indicator association with the instruction, and responsive to which,

executing while incrementing said executing. At the time the invention was made, expediting

execution using instruction cache associated with profiling was known concept. Even though

'721 does not recite receiving bundle into a instruction cache and sending the received bundle for

execution, said limitation of instruction with associated indicator would made the instruction

cache receiving and sending obvious steps within runtime based on instruction being cached in

view of the above known concept, and the incrementing responsive to association of instruction

with the indicator. The instruction in the *routine of interest* as recited by '721 is construed as

obvious representation to a runtime instruction that requires some action (e.g. to monitor or to

trace/modify leading to a counter increment in which incrementing is in terms of count of

number of executions) of the instant claims. Further, '721 does not recite 'spare bit' for indicator

identifying whether the instruction is to be monitored, but based on the indicator received into a

cache, a bit type implementation as a slot within an received instruction would have been a

obvious feature, enabling a monitoring to receive the instruction and increment a counter based

on '721 paradigm

7.   Claims 1, 32 are provisionally rejected under the judicially created doctrine of

obviousness-type double patenting as being unpatentable over claims 1, 12, 23 of copending

Application No. 10/682385 (hereinafter '385).

        As per instant claims 1, 32, '385 claims 1, 12, 23 also recite executing instructions and

detecting indicators that specify counting of events associated with the executing (Note: even

though '385 recites data values in memory specifying counting event, a runtime event such as

those memory indicators can be analogous to on runtime indicator of the instant claim); and

counting each event associated with indicators. At the time the invention was made, expediting

execution using instruction cache associated with profiling was known concept. Even though

'385 does not recite receiving bundle into a instruction cache and sending the received bundle for

execution, said limitation of executing instructions associated with indicators would made the

instruction cache reception and the sending obvious steps within runtime based on instruction

being cached in view of the above known concept, and the incrementing responsive to

association of instruction with the indicator. Even though '385 explicitly recites that counting

events associated with execution based on detection of value indicators, this limitation would be

a obvious representation of any runtime indicator that would characterizes as an event deemed

for the counter to be incremented (in which incrementing is in terms of count of number of

executions) in view of the above association determination. Further, '385 does not recite 'spare

bit' for indicator identifying whether the instruction is to be monitored, but based on the

indicator received into a cache, a bit type implementation as a slot within an received instruction

would have been a obvious feature, enabling a monitoring to receive the instruction and

increment a counter based on '385 paradigm

Claim Rejections - 35 USC § 103

8.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

9.   Claims 49-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gover et al,

USPN: 5,752,062 (hereinafter Gover), and further in view of APA (Admitted Prior Art:

Specifications/Background: pg. 3-4).

        As per claim 49, Gover discloses a computer-implemented method of monitoring

software performance in a data processing system, the computer-implemented method

comprising:

        detecting an indicator (bit … counting condition; col. 9 line 16-29; col. 10 line 40-48; col.

10 line 64 to col. 11 line 13) associated with one of an instruction and a memory location unit of

a processor; responsive to detecting the indicator, incrementing a counter (col. 11 lines 25-28

col. 12 lines 4-5, 14); and

   analyzing, in a performance monitor unit, a value of the counter to determine a

performance of the data processing system (e.g. value of the counters - col. 10 line 2-12, 16-25;

col. 11 lines 49-58; col. 14-23)

   Gover does not explicitly disclose incrementing in terms of incrementing *a counter in an*

instruction cache unit (Note: instruction cache unit treated as a intermediate stage unit acting as a

instruction processing unit located between receiving instruction being loaded from memory and

prior to sending instruction to a performance unit for execution/evaluation; i.e. no authentic

cache functionality being taught in the Disclosure regarding this "instruction cache unit") *that is*

associated with the indicator.

   Gover discloses processors (PowerPC, col. 8 lines 23-32) with special purpose registers

used to store information (see Fig. 3-4, 6-7) in a form of bit indicators stored in said special

registers, which are structurally and functionally implemented prior to the performance monitory

unit stage, and purported to enable analysis by the Performance Monitoring unit (PM) so that this

unit takes proper action; or support events (e.g. number of accesses) monitoring configuration

(e.g. MMCRn, interrupt signal - col. 9 line 52 to col. 10 line 12; col. 8 line 42 to col 9 line 26;

counts of accesses ... instruction being executed - col. 10 line 40 to col 11 line 37).   In

conjunction with a profiling mechanism (col. 10 lines 28-35) to complement analysis by the

performance monitoring process, Gover discloses count of accesses being implemented as part of

a *time base unit* (Fig. 4) via a 64-bit counter for monitoring bit flips or when a counter number of

events has occurred (col. 9 lines 10-20), based on which a notification is forwarded to the

Performance Monitoring unit 50 (e.g. *notification, interrupt condition* - col. 9 lines 21-56; Fig.

5), but Gover does not specify that the 64-bit counter is associated with an instruction loading

unit (Note: Note: instruction cache unit treated as a intermediate unit acting as a instruction

processing unit). The functionality as to monitor (by Gover's time base unit) a number of events

prior to notifying the PM 50 is reminiscent of collecting events like a profiling action (from

above) where a predefined number of events (or instructions coming from a loader) is monitored,

and profiling of program execution was well-known in the art. That is, APA teaches event-based

profiling and sample-based profiling, and according to the latter, *interruption* at some determined

intervals (see Specifications: pg. 3-4) enable recording events of interest. Based on the use of

some field or bits of special buffer to be decoded to indicate an exception or completion or a

cache miss (col 8 lined 9-12; col. 10 line 58-64) as taught by Gover's via action by instruction

dispatch unit and the monitoring for a condition (destined for the performance monitoring unit)

by a time base unit, it would have been obvious for one skill in the art at the time the invention

was made to implement condition indicator such as via the time base unit (in conjunction with

instruction loading stage) with a profiling functionality as in APA; i.e. that counter in this time

base unit operating to monitor instructions frequency as taught in APA, the event monitoring and

counter inside this unit prior to the performance monitoring unit, enabling a recorded count

indicative of a condition to support bit value such as stored in special purpose registers. One of

ordinary skill in the art would be motivated to do so because the profiling of instruction as they

are loaded and count indicator implemented inside the time base unit would provide the needed

trigger for a performance monitoring stage to take actions as taught above, e.g. the performance

monitoring unit upon receiving of such indicator, would start counting events or instruction

execution (e.g. incrementing a count of a number of times the instruction is executed) or stop if a

exception or interrupt (as in APA and Gover) due a predetermined threshold being exceeded

based on Gover's approach using fields and bit of special registers to track events.

As per claims 50-51, Gover discloses wherein responsive to the indicator being

associated with an instruction, the incrementing occurs each time an instruction is executed (refer

to the rationale of claim 49); the incrementing occurs each time the memory location unit is

accessed (see APA and rationale in claim 49, in view of: *counts of accesses ... instruction being

executed* - col. 10 line 40 to col 11 line 37; col. 17 lines 9-19).

As per claims 52-53, Gover discloses generating an interrupt from an interrupt unit

responsive to the value of the counter exceeding a threshold value (col 10 lines 42-53);

including a criteria for the counter; and generating an interrupt from an interrupt unit

responsive to meeting the criteria (col. 10 line 64-66).

Allowable Subject Matter

10.   Claims 1, 32 stand rejected in the Double patenting Rejection as set forth above; yet

contain allowable subject matter in view of the teachings provided via Fig. 31 of the

Specifications; but would be allowable if rewritten in a form including or reasonably conveying

functionality of all of the constituents of the 'instruction cache unit' described in the pertinent

section. The allowable subject matter revolves around the following scenario: A instruction

cache unit (ICU) having a counter therein that is incremented responsive to this ICU receiving of

a spare bit and an instruction, the spare bit as an indicator to be determined by the ICU as to

whether the instruction to be one to be monitored by a performance monitor unit, wherein upon

receiving a signal from the ICU in response to the determination, the performance unit

increments a counter in the ICU in conjunction with sending by the ICU of the instruction to a

functional unit.

Interview Summary

11.   The representative Thompson was initially contacted on December 23, 09 in order for the

examiner to convey whether the teachings specific to the "instruction cache unit" as proffered in

the Appeal to be recited in the scenario of the independent claims, in order to substantially

consolidate a potential allowability stead of the case. But based on the notification received on

1/04/2010 no agreement could be reached.

Conclusion

12.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Tuan A Vu whose telephone number is (571) 272-3735. The

examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

      If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Lewis Bullock can be reached on (571)272-3759.

      The fax phone number for the organization where this application or proceeding is

assigned is (571) 273-3735 (for non-official correspondence - please consult Examiner before

using) or 571-273-8300 (for official correspondence) or redirected to customer service at 571-

272-3609.

      Any inquiry of a general nature or relating to the status of this application should be

directed to the TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application
Information Retrieval (PAIR) system. Status information for published applications may be
obtained from either Private PAIR or Public PAIR. Status information for unpublished
applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR
system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Tuan A Vu/

Primary Examiner, Art Unit 2193

January 13, 2010

/Lewis A. Bullock, Jr./

Supervisory Patent Examiner, Art Unit 2193